

Reg. No:

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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations February-2022

DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 hours

Max. Marks: 60

PART-A

(Answer all the Questions 5 x 2 = 10 Marks)

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| 1 | a | Obtain the 2's complement for the number (11100011) ₂ . | 2M |
| | b | Define Encoder and Decoder. | 2M |
| | c | Draw the circuit of SR flip flop along with it's truth table. | 2M |
| | d | What is meant by Tristate logic? | 2M |
| | e | Compare PAL and PLA. | 2M |

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

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| 2 | Convert the given decimal number (234) ₁₀ to binary, octal, hexadecimal and BCD equivalent. | 10M |
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| 3 | Express the function $Y=(A+B'C)$ in (i) Canonical SOP form (ii) Canonical POS form. | 10M |
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UNIT-II

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| 4 | Minimize the given Boolean function $F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$ using tabulation method and implement using basic gates. | 10M |
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OR

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| 5 | a | Simplify the Boolean function $F(A,B,C,D)=\sum m(1,3,7,11,15)+d(0,2,5)$ using K-map | 5M |
| | b | Implement the following Boolean function with 8:1 multiplexer.
$F(A,B,C,D)=\sum m(0,2,6,10,12,13)+d(3,8,14)$ | 5M |

UNIT-III

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| 6 | What is Register Explain
i) Parallel in Parallel out Register ii) Series in Parallel out Register | 10M |
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| 7 | Draw the circuits of SR flip-flop and JK flip-flop using NAND gates and explain their operations. | 10M |
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UNIT-IV

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| 8 | What does ECL mean? Draw the circuit of Tristate ECL logic and explain the functions. | 10M |
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| 9 | Explain about CMOS families. | 10M |
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UNIT-V

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| 10 | What is RAM organization? Explain about Different types of RAM | 10M |
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OR

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| 11 | Implement PLA circuit for the following functions | 10M |
| | i) $F1(A,B,C)=\sum m(3,5,6,7)$. | |
| | ii) $F2(A,B,C)=\sum m(0,2,4,7)$. | |

END